HYB 511000AL-60/-70
1M x 1-Bit Dynamic RAM

(Low Power Version)

Advance Information

- 1 048 576 x 1-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (HYB 511000AL-60)
  70 ns access time
  130 ns cycle time (HYB 511000AL-70)
- Fast page mode cycle time
  40 ns (HYB 511000AL-60)
  40 ns (HYB 511000AL-70)
- Single +5 V (±10 %) supply with a built-in V_{BB} generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Low power dissipation
  max. 495 mW (HYB 511000AL-60)
  max. 440 mW (HYB 511000AL-70)
  max. 1.1 mW standby
- Read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden-refresh, fast page mode capability and test mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 512 refresh cycles/64 ms
- Plastic Packages:

P-DIP-18-T	HYB 511000AL
P-SOJ-26/20	HYB 511000AJL
P-ZIP-20/19	HYB 511000AZL

The HYB 511000AL-60/-70 is the new generation dynamic RAM organized as 1 048 576 words by 1-bit. The HYB 511000AL-60/-70 utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 511000AL-60/-70 to be packaged in a standard 18-pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single +5 V (±10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. These HYB 511000AL-60/-70 1M×1 DRAMs are specially selected for battery backup applications. "Test Mode" function is implemented.

Ordering Information

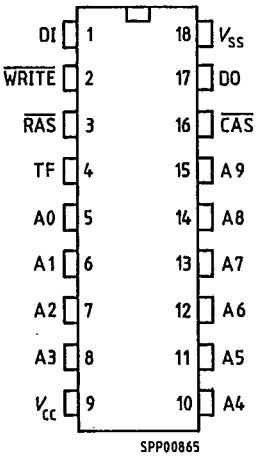
Type	Ordering code	Package	Description
HYB 511000AL-60	Q67100-Q485	P-DIP-18-T	DRAM (access time 60 ns)
HYB 511000AL-70	Q67100-Q486	P-DIP-18-T	DRAM (access time 70 ns)
HYB 511000AJL-60	Q67100-Q487	P-SOJ-26/20	DRAM (access time 60 ns)
HYB 511000AJL-70	Q67100-Q488	P-SOJ-26/20	DRAM (access time 70 ns)
HYB 511000AZL-60	Q67100-Q493	P-ZIP-20/19	DRAM (access time 60 ns)
HYB 511000AZL-70	Q67100-Q494	P-ZIP-20/19	DRAM (access time 70 ns)

Pin Names

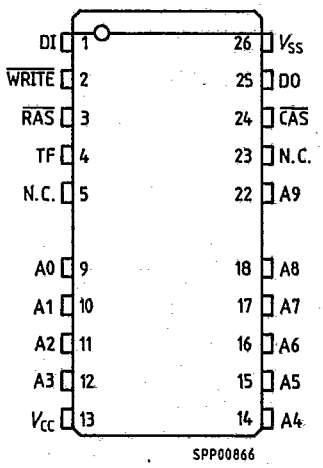
A0–A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
DI	Data Input
DO	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground (0 V)
TF	Test Function
N.C.	No Connection

Pin Configuration

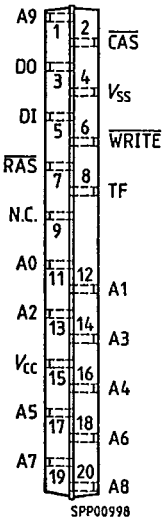
P-DIP-18-T



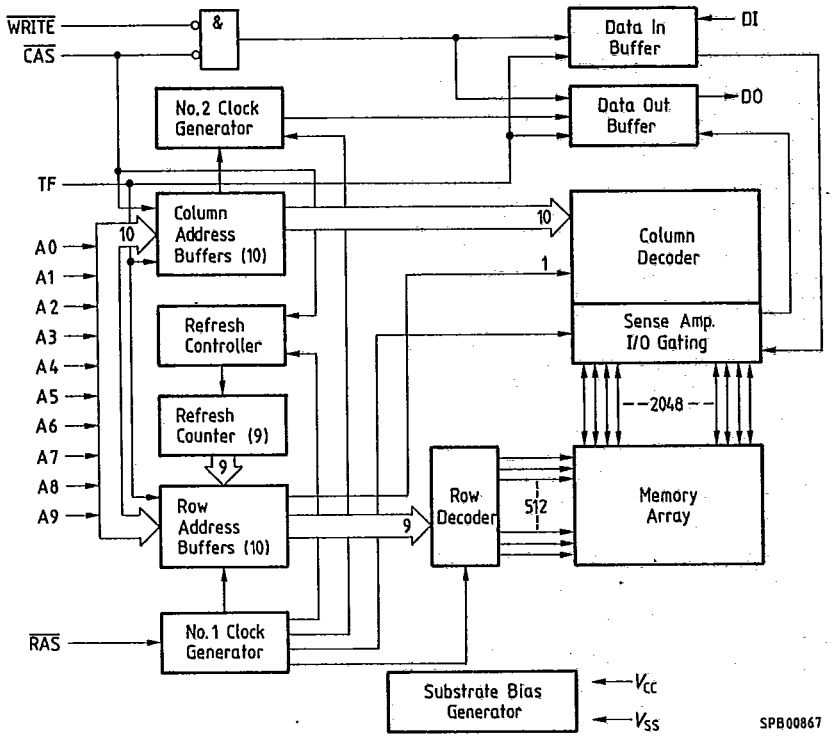
P-SOJ-26/20



P-ZIP-20/19



Block Diagram



Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range	– 55 to + 150 °C
Soldering temperature	260 °C
Soldering time	10 s
Input/output voltage	– 1 to + 7 V
Power supply voltage	– 1 to + 7 V
Power dissipation	0.6 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	–	1)
Input low voltage	V_{IL}	–1.0	0.8	V	1)
Test enable input high voltage	$V_{IH\,(TF)}$	V_{CC} + 4.5 V	10.5	V	–
Test disable input low voltage	$V_{IL\,(TF)}$	–1.0	V_{CC} + 1	V	–
Output high voltage (I_{OUT} = –5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	–10	10	µA	–
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	$I_{O(L)}$	–10	10	µA	–
Average V_{CC} supply current: HYB 511000AL-60	I_{CC1}	–	90	mA	2) 3)
HYB 511000AL-70		–	80	mA	2) 3)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					

For notes see page 6.

DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: HYB 511000AL-60	I_{CC3}	–	90	mA	2)
HYB 511000AL-70		–	80	mA	2)
($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min.)					
Average V_{CC} supply current, during fast page mode: HYB 511000AL-60	I_{CC4}	–	70	mA	2) 3)
HYB 511000AL-70		–	60	mA	2) 3)
($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling, $t_{RC} = t_{RC}$ min.)					
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC}$ –0.2 V)	I_{CC5}	–	1	mA	–
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYB 511000AL-60	I_{CC6}	–	90	mA	2)
HYB 511000AL-70		–	80	mA	2)
($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min.)					
Battery backup current average power supply current battery backup mode: ($\overline{CAS} = \overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WRITE} = V_{CC}$ –0.2 V or 0.2 V, A0 to A9 = V_{CC} –0.2 V or 0.2 V, DI = V_{CC} –0.2 V or 0.2 V or open, t_{RC} = 125 µs, $t_{RAS} = t_{RAS}$ min. ~ 1 µs)	I_{CC7}	–	300	µA	2) 13)

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

13) t_{RAS} (max.) = 1 µs is only applied to refresh of battery-backup.
t_{RAS} (max.) = 10 µs is applied to functional operating.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit values				Unit
		HYB 511000AL-60		HYB 511000AL-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Read modify write cycle time	t_{RMW}	135	–	155	–	ns
Fast page mode cycle time	t_{PC}	40	–	40	–	ns
Fast page mode RMW cycle time	t_{PRMW}	65	–	65	–	ns
Access time from $\overline{RAS}$ 6) 11)	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ 6) 11)	t_{CAC}	–	20	–	20	ns
Access time from column address 6) 12)	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge 6) 12)	t_{CPA}	–	30	–	35	ns
$\overline{CAS}$ to output in low-Z 4)	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay 7)	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) 5)	T_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100000	70	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time 11)	t_{RCD}	20	40	20	50	ns
$\overline{RAS}$ to column address delay time 12)	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50	–	55	–	ns

For notes see page 9.

AC Characteristics (cont'd) [4] [5]

Parameter	Symbol	Limit values				Unit
		HYB 511000AL-60		HYB 511000AL-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	15	–	15	–	ns
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60	–	55	–	ns
Write command pulse width	t_{WP}	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	ns
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50	–	55	–	ns
Refresh period	t_{REF}	–	64	–	64	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WRITE}$ delay time [10]	t_{CWD}	50	–	50	–	ns
$\overline{RAS}$ to $\overline{WRITE}$ delay time [10]	t_{RWD}	90	–	100	–	ns
Column address to $\overline{WRITE}$ delay time [10]	t_{AWD}	60	–	65	–	ns
$\overline{CAS}$ setup time (CBR cycle)	t_{CSR}	10	–	10	–	ns
$\overline{CAS}$ hold time (CBR cycle)	t_{CHR}	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ counter test cycle)	t_{CPN}	40	–	40	–	ns
Test mode enable setup time referenced to $\overline{RAS}$	t_{TES}	0	–	0	–	ns
Test mode enable hold time referenced to $\overline{RAS}$	t_{TEHR}	0	–	0	–	ns
Test mode enable hold time referenced to $\overline{CAS}$	t_{TEHC}	0	–	0	–	ns

For notes see page 9.

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input capacitance (A0 to A9, DI)	C_{I1}	–	6	pF	–
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, TF)	C_{I2}	–	7	pF	–
Output capacitance	C_O	–	7	pF	–

Notes for pages 7 and 8

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and the $\overline{WRITE}$ leading edge in read-write cycles.

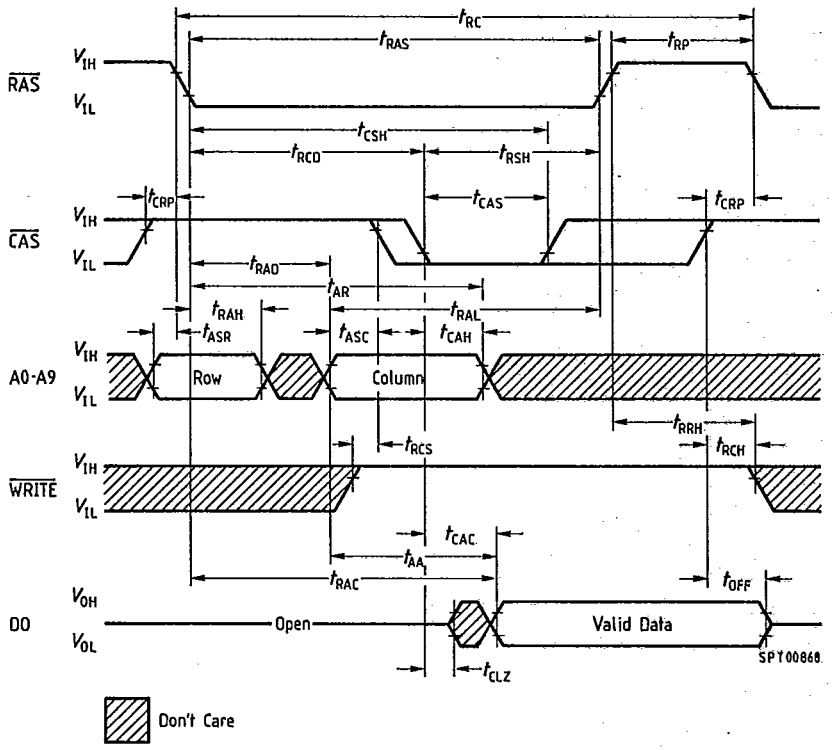
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restricted operation parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), and $t_{AWD} \geq t_{AWD}$ (min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.

11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

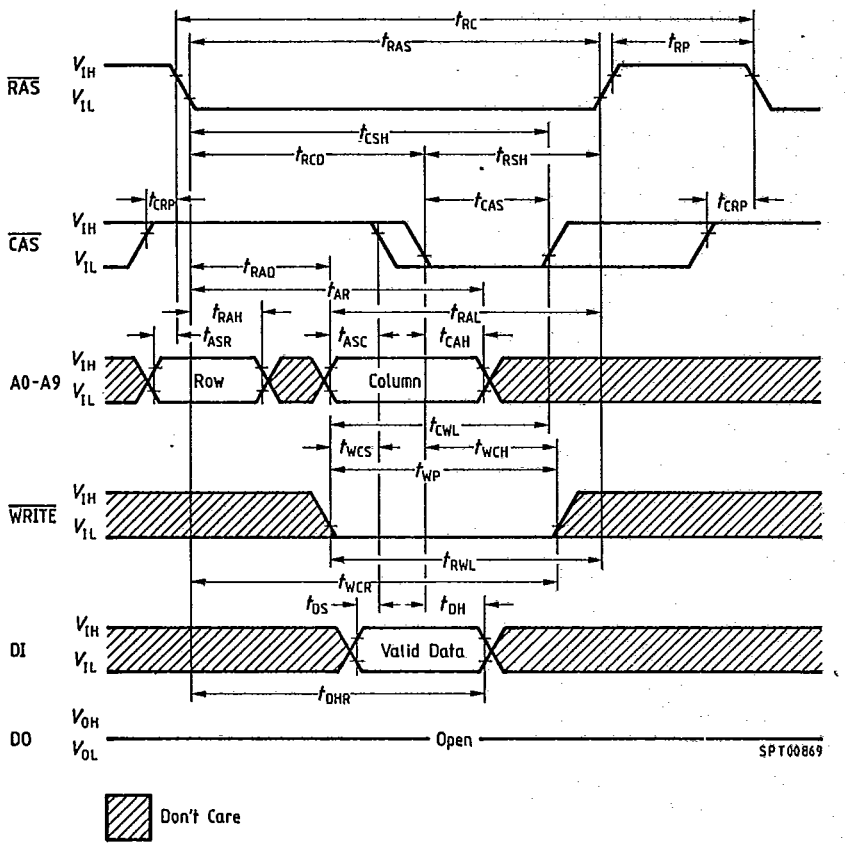
Waveforms

Read Cycle



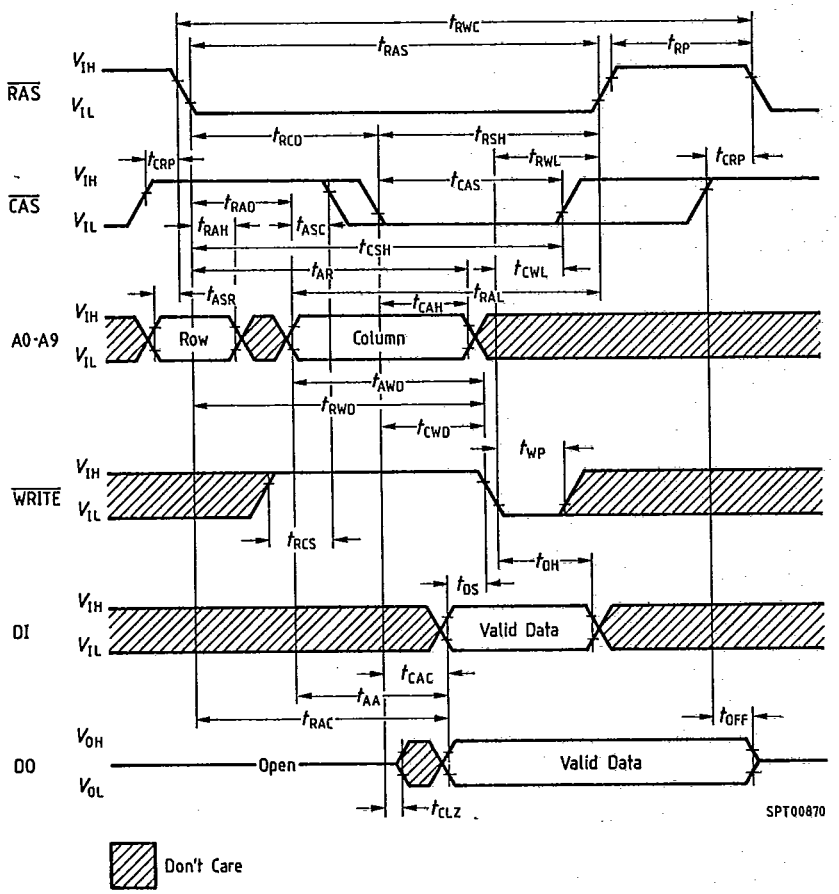
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Write Cycle (early write)



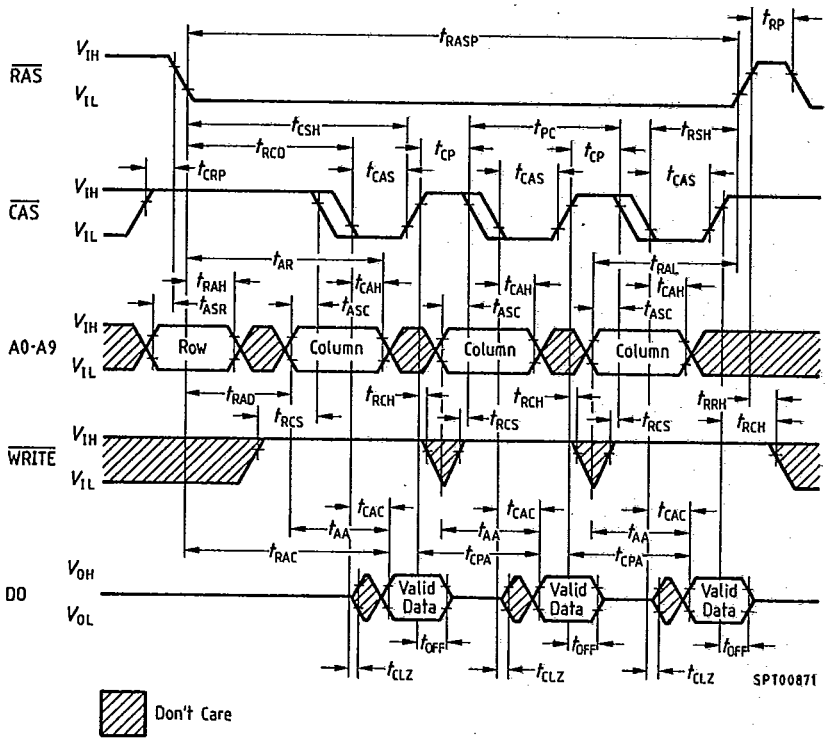
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Read-Write Cycle



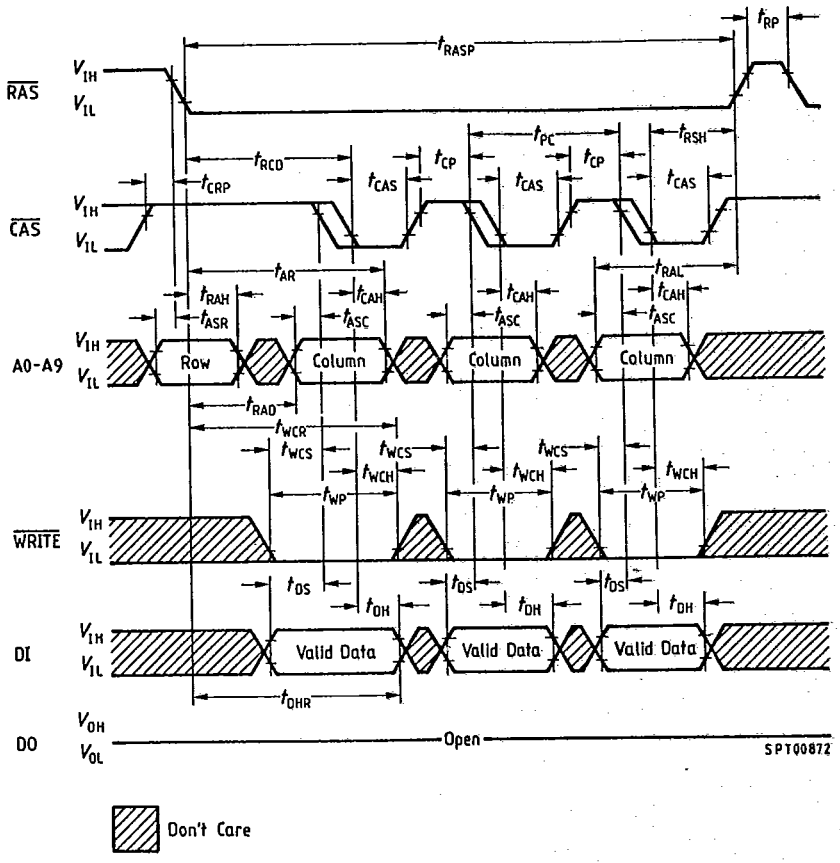
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Read Cycle



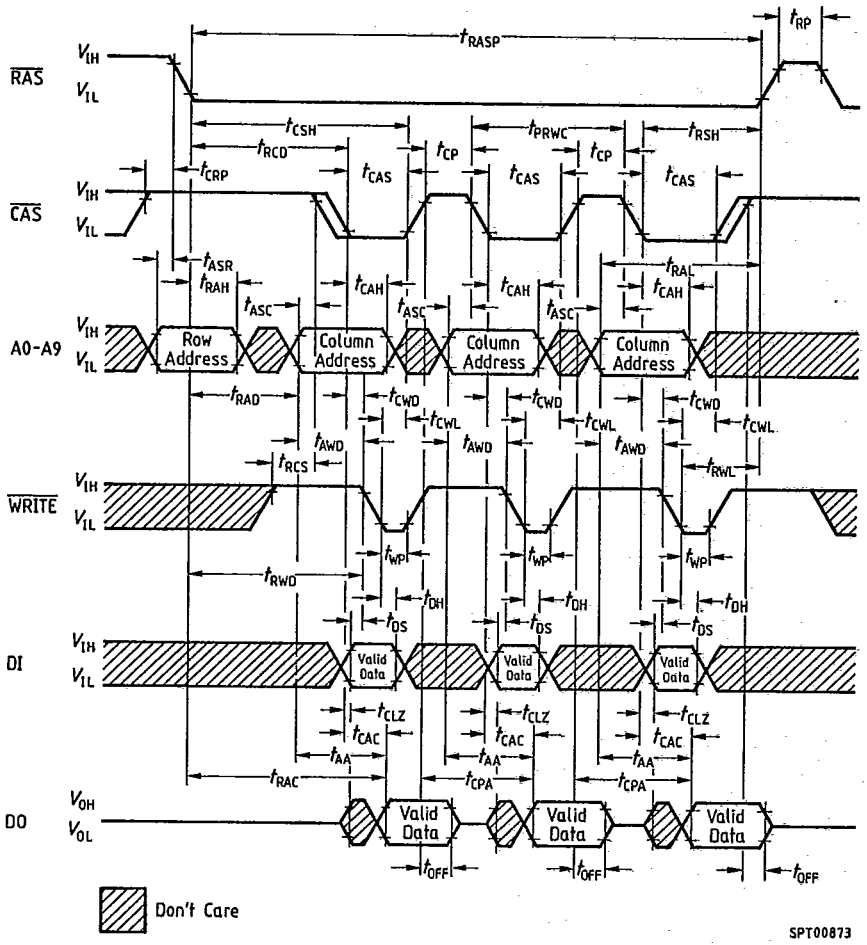
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Write Cycle (early write)



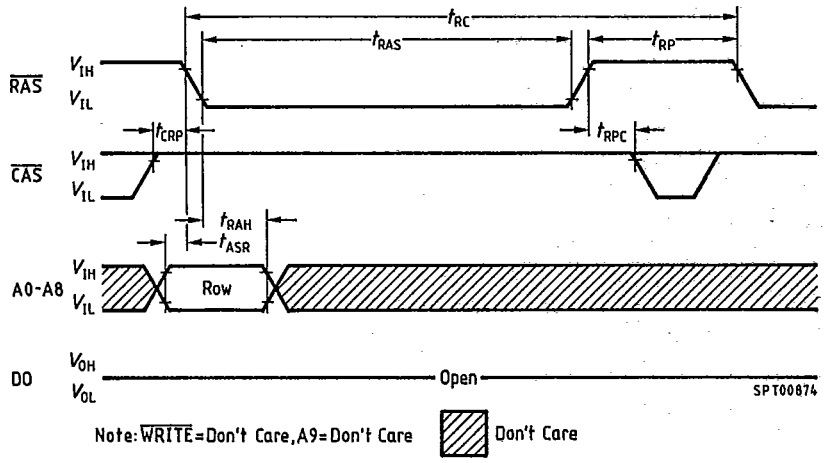
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Read-Write Cycle



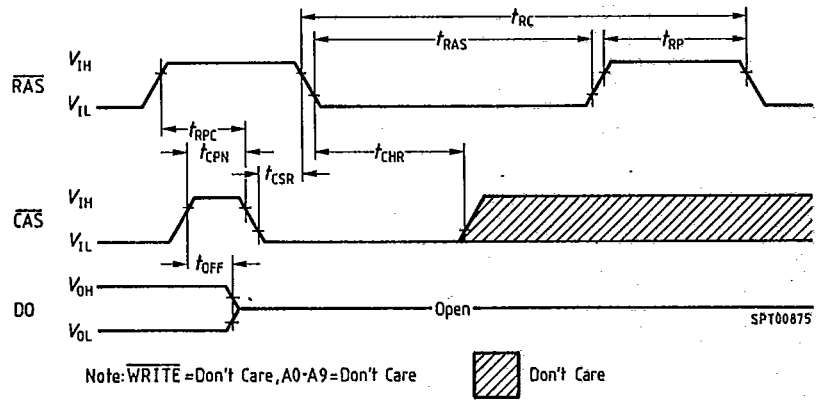
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

RAS-Only Refresh Cycle



Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

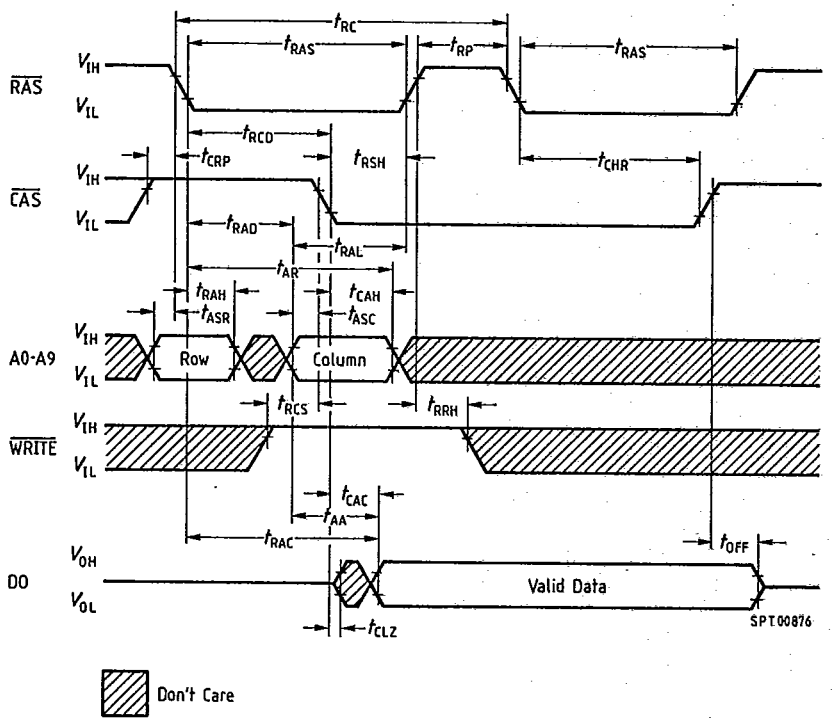
CAS-Before-RAS Refresh Cycle



Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

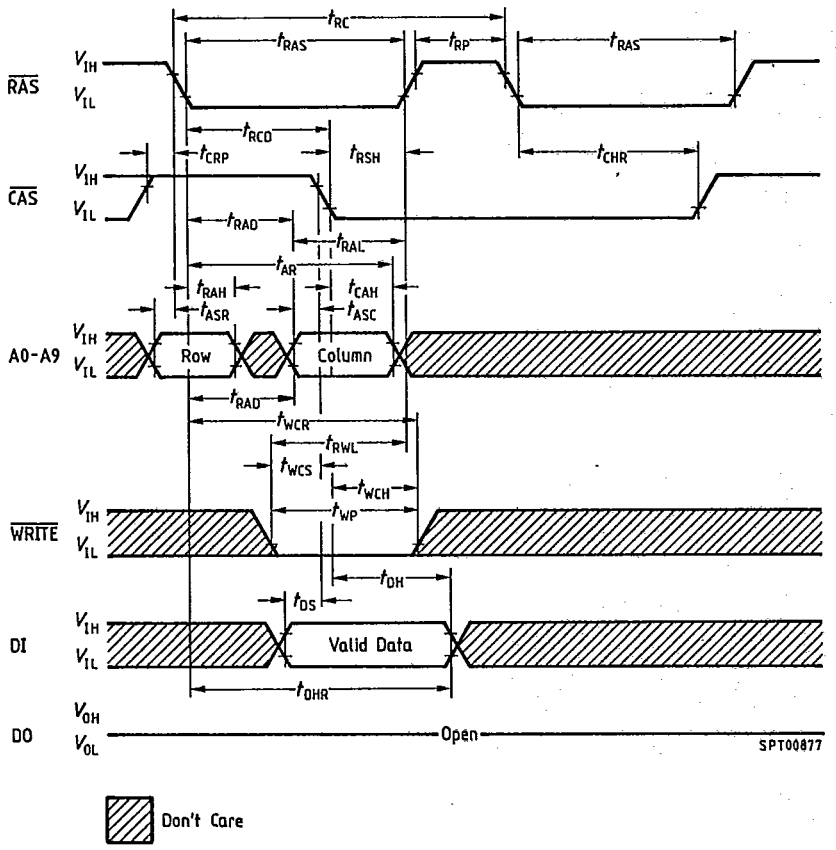
T-46-23-15

Hidden Refresh Cycle (read)



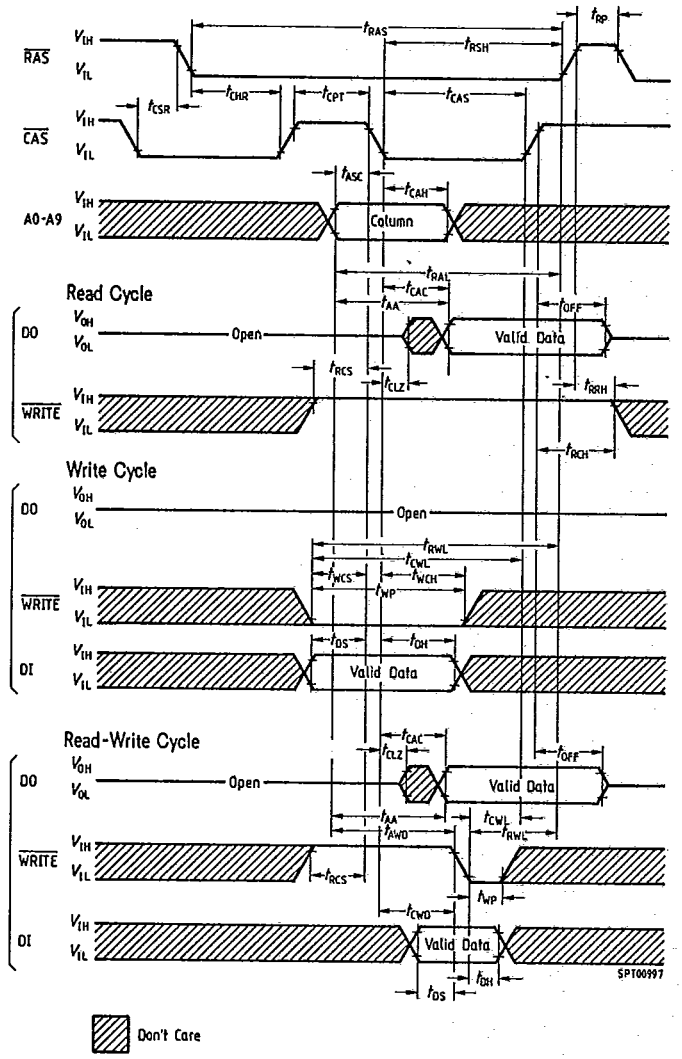
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Hidden Refresh Cycle (write)



Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

CAS-Before-RAS Refresh Counter Test Cycle

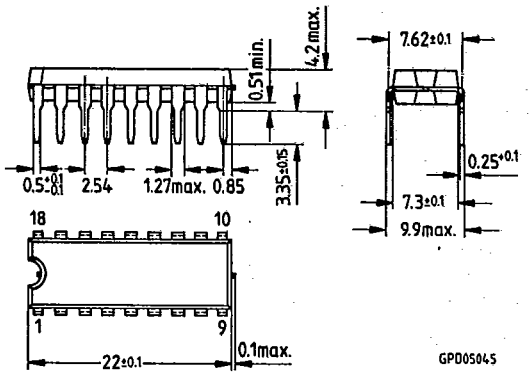


Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

T-46-23-15

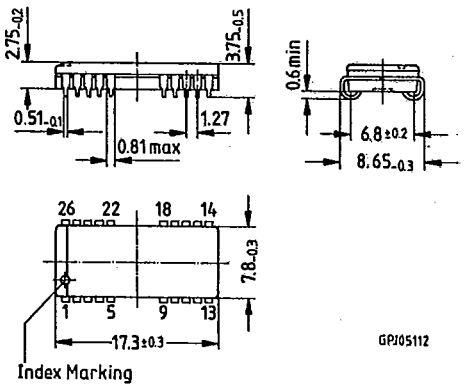
Package Outlines

Plastic Package, P-DIP-18-T
(dual-in-line-package)
20A18DIN41870T9



Dimensions in mm

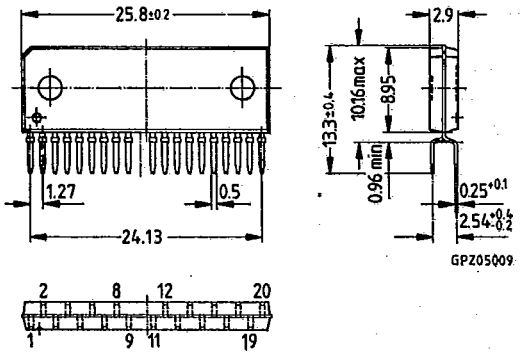
Plastic Package, P-SOJ-26/20
(Plastic small outline J-lead) - **SMD**



Dimensions in mm

Package Outlines (cont'd)

Plastic Package, P-ZIP-20/19
(JEDEC-MO-072-AA)



Dimensions in mm